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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/462,796	01/13/2000	TAKAYOSHI WATANABE	500.38090X00	5528

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/462,796	Watanabe et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 22, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2-7 and 9-33* is/are pending in the application.

4a) Of the above, claim(s) *22* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2-7, 9-21, and 23-33* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *1 and 1*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The reference submitted in the IDS (paper #13) has been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 3, 6, 7, 9, 10, 12-14, 16-18, 20, 21, 26-28 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of prior art (IDS-paper #1; Takahiro et al- Japanese Pat. 08191072) in view of prior art (IDS-paper #1; Takashi et al -Japanese Pat. 09172021 and Yoshikazu- Japanese Pat. 09148378), Yamaguchi et al (US Pat. 6271110) and Tago et al (US Pat. 5508561).

Regarding claim 2, Takahiro et al disclose a semiconductor device/circuit element having a plurality of bump electrodes with a sharp tip (Fig. 1 and 2A-E; pp. 1-5), the electrodes having a variety of shapes including pyramid (4 in Fig. 2C), prizm, etc., being formed of a conductive material/conductive resin filling up etched pyramidal or corresponding shape holes on a base material/board (Fig. 4-8) and respectively bonded

through a conductive resin film/material (3 in Fig. 1) onto pad electrodes (2 in Fig. 1 and 2) arranged on a chip/element (1 in Fig. 1 and 2).

Takahiro et al fail to specify:

a) using the base material having a crystal orientation plane, and

b) using anisotropic conductive film for bonding the electrodes

a) The prior art references (Takashi et al and Yoshikazu) teach using conventional anisotropic resin/conduction film (4 in Fig. 6, pp. 1-7 and 15 in Fig. 2; pp. 1-5 respectively) for bonding the bump and pad electrodes.

b) Yamaguchi et al teach using a base material such as a silicon plate having a crystal orientation plane (Fig. 1, 4, 6, etc.) to etch pyramidal holes to fill a conductive material in the holes (Col. 4, line 55; Col. 8, line 35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) so that the bonding strength, adhesion and bonding surface area can be improved using Yamaguchi et al, Takashi et al and Yoshikazu's bonding structure in Takahiro et al's device.

Regarding claim 6, Takahiro et al fail to specify using the bump electrodes being made of an electrode material selected from a group consisting Nickel (Ni) and copper (Cu).

However, Takahiro et al further disclose a conventional electrode structure and a mounting structure having:

- electrodes being made of a base material comprising gold (Au) bonded using a thermal compression method (Fig. 17; pp. 1-5) but and
- the mounting structure enabling the semiconductor element/device to be mounted on a substrate (25 in Fig. 17) by soldering/bonding the bump electrodes onto the terminals (26 in Fig. 17) formed on the substrate.

Tago et al disclose a semiconductor device (Fig. 14B; Col. 9, line 40- Col. 10, line 32) having a plurality of bump electrodes (6a/4a/4b; Col. 7, line 19- Col. 7, line 63) bonded by thermal compression (Col. 7, line 35) onto pad electrodes (2 in Fig. 14B) arranged on the semiconductor chip (1 in Fig. 14B). Tago et al further disclose the bump electrodes being made of a conventional material selected from a group consisting copper (Cu), Nickel (Ni), gold (Au), etc. (Col. 9, line 40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select bump electrodes being made of an electrode material selected from a group consisting Nickel (Ni) and copper (Cu) so that the desired bonding strength and hardness can be achieved using Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu's bonding structure in Takahiro et al's device.

Regarding claims 3 and 7, the claim elements have been addressed in the rejections as explained above for claims 2 and 6.

Regarding claim 9, Takahiro et al fail to specify a mounting structure enabling the semiconductor device to be mounted on the substrate by bonding the pyramidal bump electrodes on the substrate.

However, as explained above for claim 2, Takahiro et al further disclose a conventional mounting structure enabling the semiconductor device to be mounted on the substrate.

Tago et al further disclose a mounting structure comprising:

- a semiconductor device (Fig. 14B; Col. 9, line 40- Col. 10, line 32) having a plurality of bump electrodes (6a/4a/4b; Col. 7, line 19- Col. 7, line 63) bonded by thermal compression (Col. 7, line 35) onto pad electrodes (2 in Fig. 14B) arranged on the semiconductor chip (1 in Fig. 14B), and

- the mounting structure enabling the semiconductor device to be mounted on a substrate (5 in Fig. 14B) by bonding the bump electrodes onto the terminals (26 in Fig. 14B) formed on the substrate using processes such as soldering (Col. 10, line 27) or using an adhesive/conductive resin (Col. 10, line 24) to bond the bump electrodes to the terminals formed on the substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a mounting structure enabling the semiconductor device to be mounted on the substrate by bonding the pyramidal bump electrodes on the substrate so that the desired assembly interconnections can be achieved using Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu's bonding structure in Takahiro et al's device.

Regarding claim 20, the claim elements have been addressed in the rejection as explained above for claim 6.

Regarding claims 10 and 21, the claim elements have been addressed in the rejections as explained above for claims 3, 9 and 6 respectively.

Regarding claims 12 and 26, the claim elements have been addressed in the rejections as explained above for claims 3, 9 and 6 respectively.

Regarding claims 13 and 27, the claim elements have been addressed in the rejections as explained above for claims 9, 12 and 6 respectively.

Regarding claims 14 and 28, the claim elements have been addressed in the rejections as explained above for claims 3, 9 and 6 respectively.

Regarding claims 16 and 30, the claim elements have been addressed in the rejections as explained above for claims 3, 9 and 6 respectively.

Regarding claims 17 and 31, the claim elements have been addressed in the rejections as explained above for claims 2, 9 and 6 respectively.

Regarding claims 18 and 32, the claim elements have been addressed in the rejections as explained above for claims 3, 9 and 6 respectively.

3. Claims 4, 11, 15, 19, 23, 25, 29 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art (IDS-paper #1; Takahiro et al- Japanese Pat. 08191072) in view of prior art (IDS-paper #1; Takashi et al -Japanese Pat. 09172021 and Yoshikazu- Japanese Pat. 09148378), Yamaguchi et al (US Pat. 6271110), Tago et al (US Pat. 5508561) and further in view of Hosomi et al (US Pat. 6049130).

Regarding claim 4, as explained above for claims 2 and 3, Takahiro et al in view of Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu fail to specify that an alloy

can be formed at the junction of the bump and pad electrodes by using thermal compression method.

Hosomi et al teach forming bumps using conventional thermal compression method where a layer comprising an alloy such as Au/Sn (9/8 in Fig. 20; Col. 1, line 45-Col. 2, line 68) is formed at the junction due to intermetallic diffusion.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the bumps where an alloy can be formed at the junctions of the bump and pad electrodes by using thermal compression method and the bonding strength can be improved using Hosomi et al's alloy in Takahiro et al's device in view of Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu.

Regarding claim 23, the claim elements have been addressed in the rejection as explained above for claim 6.

Regarding claims 11 and 25, the claim elements have been addressed in the rejections as explained above for claims 4, 9 and 6 respectively.

Regarding claims 15 and 29, the claim elements have been addressed in the rejections as explained above for claims 4, 12 and 6 respectively.

Regarding claims 19 and 33, the claim elements have been addressed in the rejections as explained above for claims 4, 9 and 6 respectively.

4. Claims 5 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art (IDS-paper #1; Takahiro et al- Japanese Pat. 08191072) in view of prior art (IDS-paper #1; Takashi et al -Japanese Pat. 09172021 and Yoshikazu- Japanese Pat. 09148378), Yamaguchi et al (US Pat. 6271110), Tago et al (US Pat. 5508561) and further in view of Chigawa et al (US Pat. 6172422).

Regarding claim 5, as explained above for claims 2 and 3, Takahiro et al in view of Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu fail to specify bonding the bump electrode onto rewired metal conduction pads electrically connected to pad electrodes arranged on a semiconductor chip.

Chigawa et al teach bonding bump electrodes onto rewired conductive/metal substrate pad (6a/6 in Fig. 32A-34C; Col. 14, line 44; Fig. 38) which are electrically connected to pad electrodes arranged on a semiconductor chip.

The cited reference by Owada et al (US Pat. 5027188) teach using conventional rewired metal/connection pads (42 in Fig. 6; Col. 7) on the substrate (41 in Fig. 6) for a flipchip bonding.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the bump electrodes being bonded onto rewired metal conduction pads electrically connected to pad electrodes arranged on a semiconductor chip so that the routing and interconnection capability can be improved using Chigawa et al's wiring design in Takahiro et al's device in view of Tago et al, Yamaguchi et al, Takashi et al and Yoshikazu.

Regarding claim 24, the claim elements have been addressed in the rejection as explained above for claim 6.

Response to Arguments

5. Applicant contends that the restriction requirement for the method claim 22 is not proper.

However, as explained in the previous office action (paper # 6 and 12), the pyramidal holes in a base can be formed using another materially different process such as laser etching instead of photolithographic etching. Therefore, the restriction requirement is proper.

6. Applicant's arguments with respect to claims 2-7, 9-21 and 23-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

09-19-02

Steven Loke

Steven Loke